REMARKS

Claims 1-10 were previously pending in this application.

Claims 1-10 stand rejected.

Claim 1 is amended. New claim 18 is added. Support for added limitations can be found in the specification at page 6, lines 30-page 7, line 3 and FIG. 3-7 of the present application. MPEP 2163.06 states that: "[I]nformation contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter. Also, it is held in *In re Wolfensperger*, 302 F.2d 950, 133 USPQ 537 (C.C.P.A. 1962) that drawings may provide an adequate written description of the invention in the event the written disclosure portion of the application inadvertently omitted such as written description. Therefore, because the added limitations are clearly shown in FIGS. 3-7 of the instant application, no new matter has been introduced to the instant application. One of ordinary skill in the art would know what is meant by the added limitations in view of FIGS. 3-7 and the accompanying text. Thus, no new matter is added.

Claims 1-10 and 18 remain in the case.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Rejections – 35 USC § 103

Claims 1-10 are rejected under 35 U.S.C. 103(a0 as being unpatentable over the combination of (U.S. Patent No. 6,319,794) Akatsu et al., ("Akatsu et al.") and (U.S. Patent No. 6,294,823) Arafa et al., ("Arafa etal."), and further in view of (U.S. Patent No. 6,373,119) Noda ("Noda").

The rejections are respectfully traversed.

To facilitate the allowance of this case, claim 1 is amended to recite,

"a device isolation region formed in a predetermined region of the semiconductor substrate, the device isolation region having a protrusion that is higher than the top surface of the semiconductor substrate, *the protrusion, in cross section, having a sidewall that forms an obtuse angle with the top surface,*

an etch stop spacer formed overlying the sidewall of the protrusion."

In the claimed invention, because the protrusion, in cross section, has a sidewall that forms an obtuse angle with the top surface of the semiconductor substrate, an etch stop spacer

can be adequately formed on the sidewall of the protrusion. Due to this etch stop spacer 69b, the edge portion of the device isolation region 61 adjacent to the impurity diffusion region 72 is not recessed during the formation of the borderless contact holes. See page 7, lines 23-33 of the present application.

None of the cited references teach or suggest the above limitations of claimed invention. Instead, in Akatsu, the sidewall of the protrusion and the substrate surface forms an *acute* angle, not an obtuse angle. Even if an etching stop spacer were formed on the sidewall of the protrusion in the Akatsu invention, the etching stop spacer would not be adequately formed or deposited on the sidewall. This is because the acute angle would obstruct the deposition of the spacer formation layer on the protrusion. What is more, even if Akatsu and Arafa were combined, the resulting isolation structure would not be properly protected, i.e., the edge portion of the device isolation region adjacent to the impurity diffusion region would be recessed as the top portion of the resulting isolation structure would be exposed to the etching process. See FIG. 11-13D of Akatsu.

Further, Akatsu is not directed to a borderless contact hole formation technique unlike the claimed invention and is merely directed to forming a divot-free trench isolation structure that includes un-annealed dielectric material as the trench fill material. See the abstract of Akatsu. Nothing in Akatsu suggests a need to prevent the formation of a recessed device isolation region, which is a problem in a borderless contact hole formation technique. Thus, there is no suggestion or motivation to modify Akatsu with the etching stopper of Arafa to prevent the edge portion of the device isolation region adjacent to the impurity diffusion region from being recessed during the formation of the borderless contact holes.

Thus, the cited references, either alone or in combination, do not teach or suggest all of the limitations of claim 1. Accordingly, the rejection does not present a *prima facie* case of obviousness. Therefore, claim 1 is allowable and claim 2-10, which depend therefrom and recite features that are neither taught nor disclosed in the cited references, are also allowable. For example, in Akatsu, the intersection of the structure and the semiconductor surface in which it is formed, is free of silicon nitride. However, according to one embodiment of the claimed invention, an etching stop spacer etch stop spacer comprises silicon nitride or silicon oxynitride.

Additionally, for the reasons discussed above, new claim 18, which recite the limitations similar to claim 1, are also allowable.

For the foregoing reasons, reconsideration and allowance of claims 1-10 and 18 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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